Two-Stage Charge Transfer Pixel Using Pinned Diodes for Low-Noise Global Shutter Imaging

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***Abstract*— This paper describes a new type of global electronic shutter pixel for CMOS image sensors. A global electronic shutter is necessary for imaging fast-moving objects without motion blur or distortion. The proposed pixel has two potential wells with pinned diode structure for two-stage charge transfer that enables a global electronic shuttering and reset noise canceling.**

A prototype high-speed image sensor fabricated in 0.18μm standard CMOS image sensor process consists of the proposed pixel array, 12-bit column-parallel cyclic ADC arrays and 192-channel digital outputs. The sensor achieves a good linearity at low-light intensity, demonstrating the perfect charge transfer between two pinned diodes. The input referred noise at the pixel level is measured to be 6.3 e^-, which is three to four times smaller than that of conventional CMOS image sensors with global electronic shutter pixels.

***Index Terms*— CMOS image sensor, Global electronic shutter, High-speed, two-stage charge transfer, reset noise canceling.**

I. Introduction

A global electronic shutter, with which all pixels start and end integration at the same time, is necessary for imaging fast-moving objects without motion blur. CMOS image sensors with the global shuttering function are required for many applications such as high-speed cameras, automotive and industrial applications. To realize a global electronic shutter in CMOS image sensors, two kinds of techniques are reported. One uses a five-transistor (5T) pixel [1], [2]. This 5T pixel with one additional transistor for shuttering to a 4T pixel of CMOS image sensors has very simple structure, but it is difficult to attain low noise performance, because of the large reset noise caused by the use of floating diffusion as an analog memory for global shuttering. The other uses a charge amplifier and sample-and-hold circuits in each pixel [3]. This pixel can reduce reset noise and enhance the sensitivity by the charge amplifier. However, this pixel has large pixel size due to the complicated circuits.

This paper presents a new type of global electronic shutter pixel. The proposed pixel features two-stage charge transfer using different-depth potential wells in two pinned diodes. Using this structure, the reset noise at the floating diffusion can be canceled by the true correlated double sampling(CDS) operation, while attaining a global shuttering function. The pinned diode structure prevents signal electrons to be captured at Si-SiO_2 interface traps and reduces the resulting image lag and charge transfer noise[4]. As a result, very low noise level when compared with the conventional global shutter pixels is expected. Furthermore, dark current is also reduced with the pinned diode structure.

II. Proposed Pixel

A. Structure and Operation

Fig.1 shows the proposed pixel structure and potential profile. The pixel has two pinned diodes: photodiode (PD) and storage diode (SD). For perfect charge transfer between the two pinned diodes, voltage difference V_D is necessary. The V_D is built by slit-shaped PD structure shown in Fig.3 [5]. It can be implemented with a standard CMOS image sensor technology, without any special processing steps. The SD and a floating diffusion (FD) which has a role of charge detection are connected with a transfer gate TX. The voltage change of the FD due to transferred photo-charge is read out through a source follower amplifier. To reduce the number of transistors in a pixel, a floating diffusion driving technique [6] is used. Fig.2 shows the timing diagram of the proposed pixel. The operation at the beginning of a frame is as follows. First, an accumulated charge in the PD is transferred to the SD as a first transfer. The first transfer realizes a global electronic shutter function. If the first transfer is not perfect, some amount of charge is left in the PD. The residual charge causes image lag and noise. Therefore, the PD is reset through GR gate and consequently the residual charge is drained. After that, all the pixel signals are read out. To readout the signal, each horizontal pixel line is selected by sequentially setting V_R to high level, and then the FD of the selected pixel is reset. The reset level is read out through a buffer amplifier. Then, the signal charge is transferred from the SD to FD as a second transfer and the resulting signal voltage in the FD is read out. By taking the difference between the reset and signal levels, the reset noise and the fixed pattern noise are cancelled.

B. Simulation Results

Simulation results of potential distribution(x-x' direction) by changing GS gate voltage are shown in Fig.4. Larger V_D leads to a higher charge transfer efficiency. The maximum V_D, however, is limited by the minimum width of n-type region which is determined by the design rule of fabrication technology. In the layout shown in Fig.3, V_D of 0.2V is obtained using the smallest width of n-type region. The slit-shaped PD structure may not be efficient if large amount of electrons must be stored for attaining wide dynamic range.

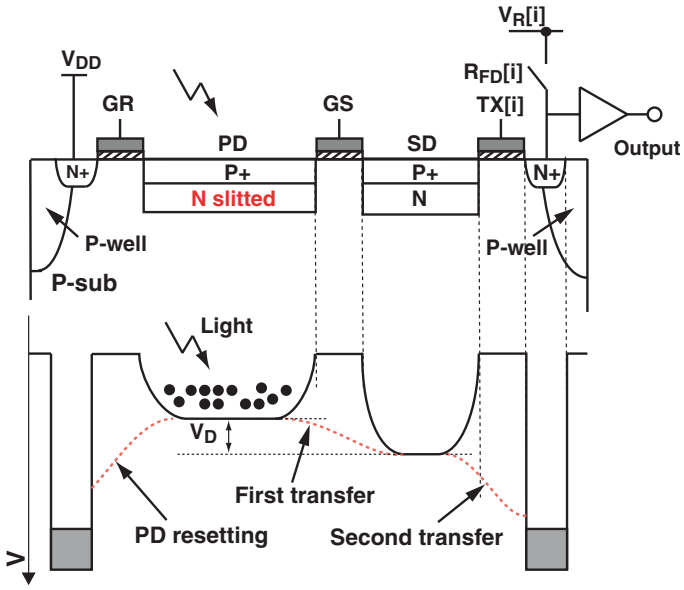

Fig. 1. Proposed pixel structure and potential profile

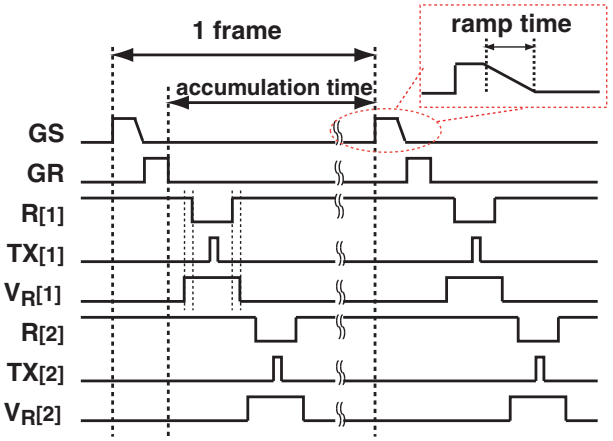

Fig. 2. Timing diagram

In the designed slit-shaped structure, the saturation number of electrons is 18000e$^-$ according to a simulation result. This value is sufficiently large when compared with those of recent CMOS image sensors.

Fig.5 shows the simulation results of the residual charge as a function of the accumulated charge in the PD. The horizontal and vertical axes represent the number of accumulated electrons in the PD before the first charge transfer and the number of residual electrons in the PD, respectively. In this simulation, the falling edge of the input pulse of the GS gate is ramped to increase the charge transfer efficiency(Fig.2). This result indicates that the residual charge depends on the accumulated charge and a perfect charge transfer is possible when the accumulated charge is small. Therefore the sensitivity degradation does not occur at low-light intensity. Since the residual charge due to the incomplete charge transfer is drained through the GR gate, image lag can be avoided.

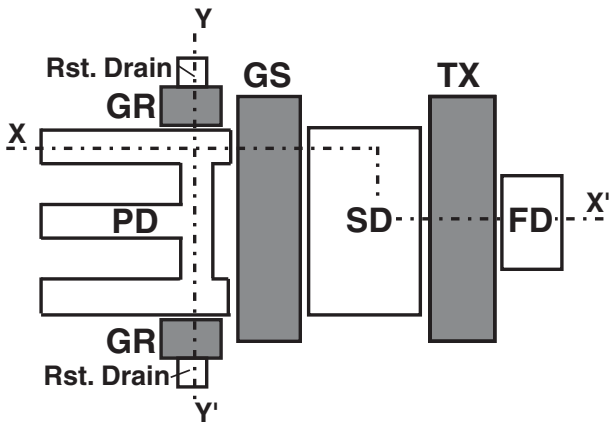

Fig. 3. Pixel layout

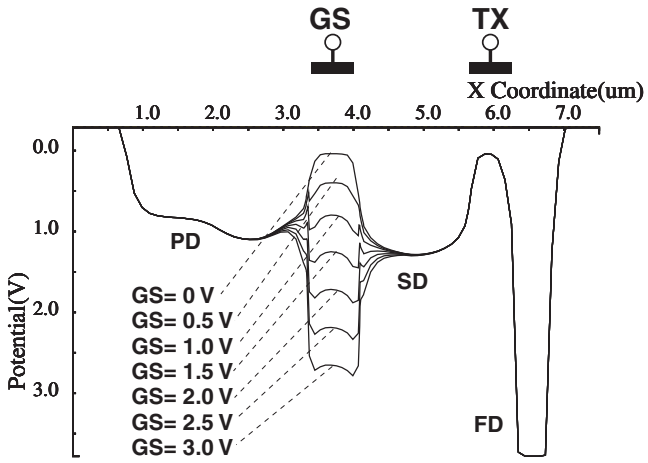

Fig. 4. Potential distribution at the first charge transfer (x-x')

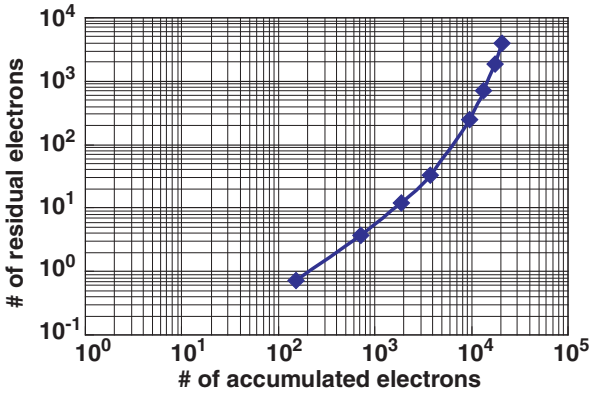

Fig. 5. the dependency of the residual charge on the accumulated charge in PD

III. Experimental Results

A prototype high-speed CMOS image sensor with the proposed pixel is designed and implemented. A chip photograph of the developed high-speed image sensor with 0.18-μm one poly four-metal standard CMOS image sensor technology is shown in Fig.6. The image array has 1024 $\times$ 1024 pixels with the pixel pitch of 7.5μm. The chip size is 10mm $\times$ 13mm.

Two 512 cyclic ADC arrays [3] are integrated at the upper and lower sides of the image array. The sensor has the digital parallel output of 192 channels.

Fig.7 shows output characteristics of the image sensor. The image sensor output range of 0 to 1V is assigned to the half of 12 bit digital code range, i.e., 0 to 2047. The sensor output has obviously large nonlinearity at high light intensity when compared with a linear line whose gradient is fitted to the measured result at the origin. As Fig.5 predicts the incomplete charge transfer in high light intensity region causes a large residual charge, and the resulting nonlinearity. On the other hand, the output has a good linearity at low light intensity, showing that perfect charge transfer can be achieved for the relatively small number of accumulated electrons in the PD. The nonlinearity at high light intensity can be an issue for some application, but Larger V_D can improve the charge transfer characteristic and thereby results in a good linearity. The Larger V_D can be created by controling doping profiles of PD and SD independently, which requires additional processing steps to a standard CMOS image sensor technology.

Table I summarizes the performance of the sensor. The input referred noise of the sensor, including the pixel and column cyclic ADC is measured to be 81 e^-. The random noise of the cyclic ADC only is 78 e^-. Therefore random noise of the sensor is dominated by the column cyclic ADC. This large noise is due to the digital switching noise for the high-speed digital readout. This noise has to be reduced in the future design. To measure the essential pixel noise, the analog output to directly read out the pixel output, is measured by an off-chip 14-bit ADC. The input referred noise of the pixel only is measured to be 6.3 e^-. The equivalent number of noise electrons due to reset noise $\overline{N_{n,reset}}$ is given by

$$\overline{N_{n,reset}} = \sqrt{\frac{V_{th}}{G_C}} \quad (1)$$

where V_{th} is the thermal voltage, which is 25.9mV at 27 °C . The conversion gain G_C is measured to be 33 μV/e^-. Therefore $\overline{N_{n,reset}}$ is calculated to be 28 e^- and it increases to 40 e^- after the readout in case of the uncorrelated double sampling in a conventional 5T global shutter pixel. The achieved noise level of 6.3 e^- in the proposed structure where the reset noise can be canceled is smaller than 1/6 of the conventional global shutter pixel. The input referred noise of the pixel is three to four times smaller than the conventional CMOS image sensor with the a global electronic shutter function [2].

As shown in Table I, the dark current of the proposed pixel is measured to be 284e^-/sec at ambient temperature of 18 °C . This dark current level of the proposed pixel is much smaller than that of 5T pixels using surface PD [1]. The dark current of the proposed pixel can be further reduced by optimizing the size and structure of the PD and SD.

A sample image captured at 1000fps is shown in Fig.8. This sample image is synthesized with eight regions of an image captured separately by a logic analyzer with a large-size memory. This is because data of 24 channels only are obtained at a time due to the limitation of the experimental environment. The image indicates that the sensitivity degradation does not occur at low-light intensity. The image quality is not good enough because of the vertical fixed pattern noise and row random noise. These noises come from column cyclic ADCs and digital read circuits. These noises are not essential and can be reduced by re-examining the design details because a high-speed CMOS image sensor(512 × 512pixels, 3500fps) using almost the same ADC architecture as of the present paper has been implemented and shows a good image quality[3]. Fig.9 shows 30 consecutive frames from a video sequence captured at 1000fps. To show the motion of fast moving object("chopper blade", rotating at 15Hz), 128×144 pixels only is shown. The edge of the chopper blade has neither motion blur nor distortion, showing the effectiveness of the global electronic shutter.

Fig. 6. chip photo(10mm×13mm)

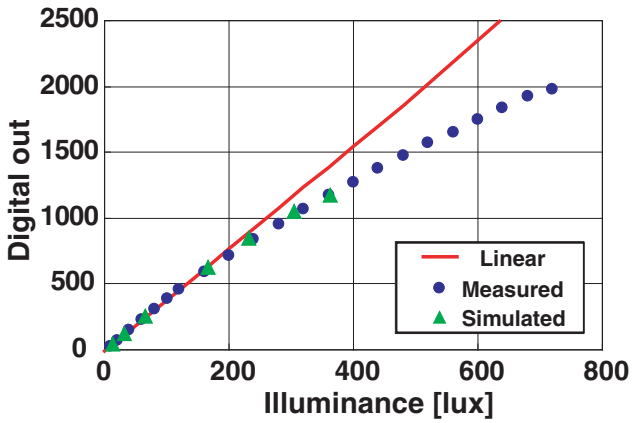

Fig. 7. output characteristic

TABLE I

PERFORMANCE SUMMARY

Technology	0.18-μm standard CIS 1P4M
Chip size	13mm(H) $\times$ 10mm(V)
Effective pixels	1024(H) $\times$ 1024(V)
Pixel size	7.5 μm $\times$ 7.5μm
Frame rate	$>$1000fps
Sensitivity	0.95 V/lux·sec
Conversion gain	33 μV/e$^-$
Random noise(sensor)	81 e$^-$
Random noise(pixel only)	6.3 e$^-$
Random noise(ADC only)	78 e$^-$
Fixed pattern noise	229 e$^-$
Dark current	284 e$^-$/sec at 18 °C
ADC resolution	12bit(Full scale $2V_{\text{peak to peak}}$)
Power supply	1.8V(Digital)/3.3V(Analog)
Power consumption	1.2W(@500fps)

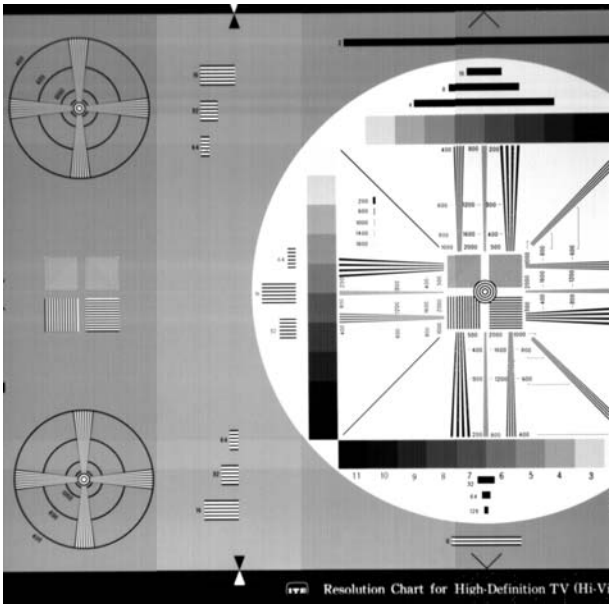

Fig. 8. Sample image at 1000fps

IV. CONCLUSIONS

In this paper, a global electronic shutter pixel which enables reset noise canceling and reduced dark current has been described. The proposed pixel has two pinned diodes that have different-depth potential wells. The voltage difference between the potential wells is generated by slitted photodiode structure. A prototype high-speed image sensor with 1M pixels is fabricated using 0.18um standard CMOS image sensor technology. The sensor achieves a good linearity at low light intensity, demonstrating the perfect charge transfer between two pinned diodes. The output characteristic of the sensor shows a good agreement with the simulation results using a device simulator. The noise measurement results indicate that the proposed pixel successfully cancels the reset noise, and the resulting input referred noise is as small as 6.3 e$^-$.

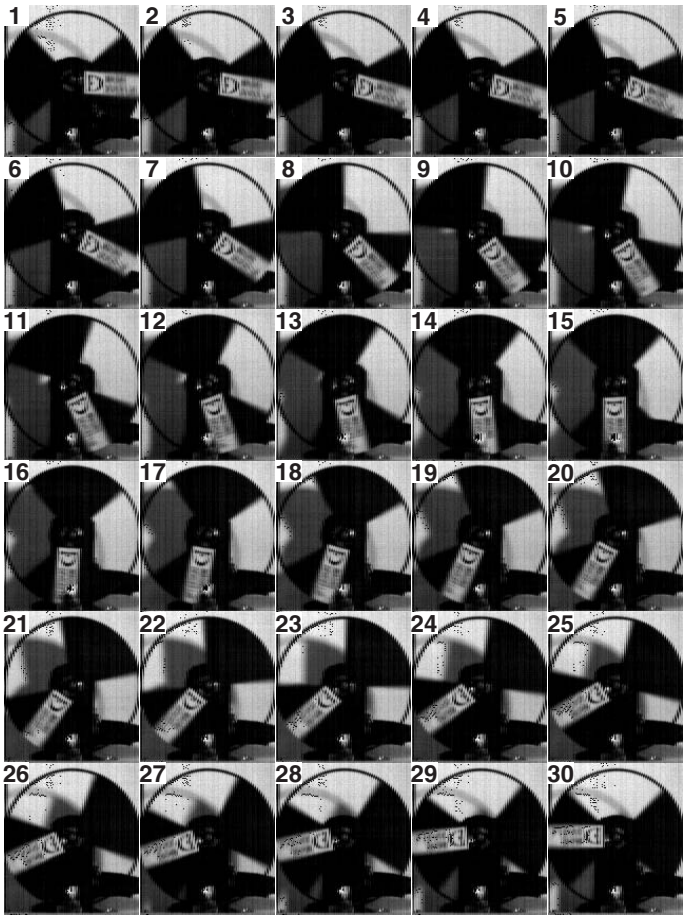

Fig. 9. Image sequence at 1000fps

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